Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VCP**
2. **A1**
3. **A2**
4. **A0**
5. **A6**
6. **A5**
7. **A7**
8. **VEE**
9. **A3**
10. **A4**
11. **D3**
12. **D2**
13. **N. CS**
14. **D1**
15. **D0**
16. **VCC**

**.116”**

**14**

**13**

**12**

**11**

**2 1 16 16 15**

**3**

**4**

**5**

**6**

**7 8 8 9 10**

**.128”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref: K6POG**

**APPROVED BY: DK DIE SIZE .116” X .128” DATE: 11/15/21**

**MFG: MOTOROLA THICKNESS .021” P/N: MCC10149**

**DG 10.1.2**

#### Rev B, 7/1